Docket No.: 065933-0081 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
Kuniyuki TANI, et al.	:	Confirmation Number: 5532
Application No.: 10/808,575	:	Tech Center Art Unit: 2816
Filed: March 25, 2004	:	Examiner: Terry D. Cunningham

For: BIAS VOLTAGE GENERATING CIRCUIT, AMPLIFIER CIRCUIT, AND PIPELINED AD CONVERTER CAPABLE OF SWITCHING CURRENT DRIVING CAPABILITIES

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is Appellant's Appeal Brief in support of the Notice of Appeal filed November 9, 2005. Please charge the Appeal Brief fee of $500.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due under 37 C.F.R. 1.17 and 41.20, and in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

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APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
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Alexandria, VA 22313-1450

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed November 9, 2005, wherein Appellant appeals from the Primary Examiner's rejection of claims 1-5, 7, 9, 11-14, 16, 18, 20 and 21.

I. REAL PARTY IN INTEREST

This application is assigned to Sanyo Electric Co., Ltd. by assignment recorded on March 25, 2004, at Reel 015144, Frame 0296.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF CLAIMS

Claims 1 through 21 are pending. Claims 1 through 5, 7, 9, 11 through 14, 16, 18, 20 and 21 stand under final rejection and are under appeal. Claims 6, 8, 10, 15,17 and 19 stand under objection.

IV. STATUS OF AMENDMENTS

No amendment has been filed subsequent to the issuance of the Final Action dated August 10, 2005 (hereinafter referred to as "the Office Action").

V. SUMMARY OF INVENTION

The claims are directed to a bias voltage generating circuit and a control circuit therefor. One of a plurality of bias voltage generating circuits 70 is illustrated in Fig. 3 and described in the specification beginning at page 10, line 11. A driving unit 80 generates a bias voltage to be applied to a load such as an amplifier of an image processor. In a period for applying the bias voltage to the load, control unit 88 switches the current driving capability of the driving unit 80 according to a variation in the amount of current necessary for the load. The driving unit 80 includes a first bias circuit 82 and a second bias circuit 84, which comprise a plurality of bias circuits that are connected in parallel. Bias circuits 82 and 84 have different current driving capabilities, but output the same bias voltage. These circuits are described in detailed at page 10, line 20 to page 12, line 8 of the specification.

Bias circuit 82 contains a CMOS transistor pair, transistor Tr1 and transistor Tr2, which are connected in series between a power supply potential VDD and a ground potential VSS. Transistor Tr1 is a P-channel MOS transistor, transistor Tr2 an N-channel MOS transistor. Transistor Tr1 and transistor Tr2 have a common drain electrode, and are diode-connected with their respective gate electrode and the drain electrode shorted. The common drain electrode outputs the voltage divided by the ON resistances of transistor Tr1 and transistor Tr2 as the bias voltage. The output node is coupled

to output transistor Tr10, a switching element for output control. Transistor Tr3 is a switching element that interrupts a feedthrough current from the CMOS transistor pair.

The second bias circuit 84 contains a similar circuit configuration. The output node of the bias voltage from the first bias circuit 82 is connected with the output node of the bias voltage from the second bias circuit 84, and led to conversion unit 22. The ratio between the device sizes of transistor Tr1 and transistor Tr2 in the first bias circuit 82 is configured the same as the ratio between the device sizes of transistor Tr4 and transistor Tr5 in the second bias circuit 84. Such size ratios are maintained while transistor Tr1 and transistor Tr2, or transistor Tr4 and transistor Tr5, are increased in size for the sake of different current driving capabilities. In general, the higher the feedthrough current, the higher the current driving capability.

The control unit 88 switches the current driving capability of the entire driving unit 80 by controlling the number of circuits to operate out of the first bias circuit 82 and the second bias circuit 84. For example, in a period when the first conversion unit 22 requires a relatively high current, both the first bias circuit 82 and the second bias circuit 84 are operated. In a period when a relatively low current is sufficient, either one of the first bias circuit 82 and the second bias circuit 84 is operated. The current driving capabilities of the first bias circuit 82 and the second bias circuit 84, and the control timing of the control unit 88 on transistor Tr3, transistor Tr6, output transistor Tr10, and output transistor Tr20 are designed in accordance with the variation in the amount of current required in the conversion unit 22 to which the bias voltage is applied.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 1 through 5, 7 and 9 are anticipated by U.S. patent 5,650,672 (hereinafter "Curd") under 35 U.S.C. § 102(b).

B. Whether claims 11 through 14, 16, 18, 20 and 21 are unpatentable over U.S. patent 6,028,546 (hereinafter "Signell") in view of Curd under 35 U.S.C. § 103(a).

VII. ARGUMENT

A. Rejection under 35 U.S.C. §102(b) over Curd.

The factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically claimed invention is placed into the recognized possession of one having ordinary skill in the art. *Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 66 USPQ2d 1801 (Fed. Cir. 2003); *Crown Operations International Ltd. v. Solutia Inc.*, 289 F.3d 1367, 62 USPQ2d 1917 (Fed. Cir. 2002). In imposing a rejection under 35 U.S.C. § 102, the Examiner is required to specifically identify wherein an applied reference is perceived to identically disclose each and every feature of a claimed invention. *In re Rijckaert*, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984). It is submitted that the burden imposed on the examiner by 35 U.S.C. § 102 as summarized in the above-identified precedents has not been discharged.

1. Claim 1

Claim 1 is an independent claim and is reproduced as follows:

> 1. A bias voltage generating circuit, comprising: a driving unit which generates a bias voltage to be applied to a predetermined load; and
>
> a control unit which switches a current driving capability of the driving unit according to a variation in an amount of current required for the load in a period for applying the bias voltage to the load.

The Office Action relies upon Fig. 2 of Curd for meeting the claimed requirements. According to the Office Action, the recited "control circuit" is purported to be disclosed by "IN and the inverter." The only description of Fig. 2 in Curd is found at column 4, lines 44-47, *i.e.*, a level shifter. None of the individual elements of the circuit of Fig. 2 bears a reference number or is discussed in the specification. The "IN" identifier is not a control circuit but merely a line connected to the gates of two FETs, one through the inverter.

The Office Action is silent as to the explicit claim requirement for switching "a current driving capability of the driving unit *according to a variation in an amount of current required for the load* in a period for applying the bias voltage to the load (emphasis supplied)." No such circuit is disclosed or suggested by Curd.

Curd merely discloses a multiplexer to selectively provide a plurality of high-voltage levels to a common conductor, such as Programmable Logic Devices, which typically make use of one or more programmable interconnect arrays to configure themselves to a specific user's design. The programmable interconnect arrays are typically composed of some type of nonvolatile, floating gate memory cell, such as an EPROM, EEPROM, flash EPROM, etc. These memory cells require a

plurality of voltage levels, some of which are high-voltage, to program, erase, and verify the cell. The level shifter of Fig. 2 is merely schematically disclosed for illustration purposes.

As Curd has no disclosure of establishing current driving capability in accordance with the load requirements, Curd fails as an anticipatory reference for claim 1.

2. Claim 2

Claim 2 is dependent from claim 1 and further requires that the driving unit include a plurality of bias circuits which are connected in parallel and have different current driving capabilities, and that the control unit switches the current driving capability by controlling the number of circuits to operate out of the plurality of bias circuits. Curd does not disclose these additional requirements, nor have they been addressed in the Office Action rejection. It is submitted, therefore, that the rejection of claim 2 fails both for the lack of disclosure in Curd of all requirements of parent claim 1 and for the additionally recited elements.

Specifically, there is nothing in the Curd disclosure of Fig. 2 of a plurality of bias circuits that have different current driving capabilities and are connected in parallel. While there are two parallel circuits shown, there is no indication in Curd that the two circuits have different current driving capabilities. Curd does not disclose a control unit that controls the *number* of circuits of the plurality of circuits that operate. Assuming, *arguendo*, that "IN" and the inverter comprise a control circuit, this combination would activate one of the parallel circuits while deactivating the other via the inverter. That is, while the circuit to be activated may be controlled, the number of circuits that are activated is not controlled.

3. Claim 3

Claim 3 is dependent from claim 1 and further requires that the driving unit include a plurality of bias circuits which are connected in parallel and have the same current driving capabilities, and that the control unit switches the current driving capability by controlling the number of circuits to operate out of the plurality of bias circuits. Curd does not disclose these additional requirements, nor have they been addressed in the Office Action rejection. It is submitted, therefore, that the rejection of claim 3 fails both for the lack of disclosure in Curd of all requirements of parent claim 1 and for the additionally recited elements.

Curd provides no discussion as to current driving capabilities of the two parallel circuits illustrated. Whether the driving capabilities are the same or different is of no concern in the Curd disclosure. As discussed in the previous section above, Curd does not disclose a control unit that controls the *number* of circuits of the plurality of circuits that operate. Assuming, *arguendo*, that "IN" and the inverter comprise a control circuit, this combination would activate one of the parallel circuits while deactivating the other via the inverter. That is, while the circuit to be activated may be controlled, the number of circuits that are activated is not controlled.

4. Claim 4

The rejection of claim 4 fails with respect to the requirements of its parent claim 1, for the reasons presented above. Claim 4 additionally requires that the predetermined load is an amplifier which is included in an AD converter. Curd does not disclose this requirement either. The load disclosed by Curd is a multiplexer.

5. Claim 5

Claim 5 is dependent from claim 2. The rejection of claim 5 fails with respect to the requirements of its parent claims 2 and 1 for the reasons presented above.

Claim 5 additionally requires that "*each* of the plurality of bias circuits includes . . . a CMOS transistor pair composed of a PMOS transistor and an NMOS transistor which are connected in series between a power supply potential and a ground potential and have a common drain connected to their respective gates, the drain outputting the bias voltage . . . ." This requirement is not addressed in the Office Action, which has relied upon the Fig. 2 disclosure for the rejection. Fig. 2 does not illustrate a plurality of bias circuits, each including a CMOS pair as required by claim 5. Lack of such disclosure is an additional basis upon which it is submitted that the rejection is untenable.

7. Claim 7

Claim 7 is dependent from claim 5. The rejection of claim 7 fails with respect to the requirements of its parent claims 5, 2 and 1 for the reasons presented above.

Claim 7 additionally requires that the control unit controls the number of circuits to operate by sending control signals to the respective switching elements included in the plurality of bias circuits. Curd lacks disclosure of this additional feature, another basis for withdrawal of the rejection.

9. Claim 9

Claim 9 is dependent from claim 1. The rejection of claim 9 fails with respect to the requirements of its parent claim 1 for the reasons presented above.

Claim 9 additionally requires, in part, that the control unit switches the output of the driving unit between a first bias voltage and a second bias voltage according to a variation in the amount of current necessary for the load. Curd does not disclose this feature, nor has this requirement been addressed in the Office Action.

B. Rejection of claims 11 through 14, 16, 18, 20 and 21 over Signell in view of Curd under 35 U.S.C. § 103(a).

Legal precedent is well developed on the subject of obviousness in the application of a rejection under 35 U.S.C. §103. It is incumbent upon the examiner to factually support a conclusion of obviousness. *In re Mayne,* 104 F.3d 1339, 41 USPQ2d 1451 (Fed. Cir. 1997*); In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). The examiner must provide a reason why one having ordinary skill in the art would have been led to modify a particular prior art reference in a particular manner to arrive at a particular claimed invention; *Ecolochem Inc. v. Southern California Edison, Co.* 227 F.3d 361, 56 USPQ2d 1065 (Fed. Cir. 2000); *In re Rouffet*, 149 F.3d 1350, 47 USPQ2d 1453 (Fed. Cir. 1998). *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *In re Warner*, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967).

In order to establish the requisite motivation, "clear and particular" factual findings must be made as to a specific understanding or specific technological principle which would have realistically compelled one having ordinary skill in the art to modify a particular reference to arrive at the claimed invention based upon facts-- not generalizations. *Ruiz v. A.B. Chance Co.*, 234 F.3d 654, 57 UPSQ2d 1161 (Fed. Cir. 2000); *Ecolochem Inc. v. Southern California Edison, Co.* 227 F.3d 361, 56 USPQ2d 1065 (Fed. Cir. 2000); *In re Kotzab*, 217 F.3d 1365, 55 USPQ 1313 (Fed. Cir. 2000); *In re Dembiczak*,

175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999). What may or may not be known in general does not establish the requisite realistic motivation for obviousness; see *In re Deuel*, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995).

1. Claims 11, 20 and 21

Claims 11 and 20 are independent and recite, *inter alia*, "a control unit which switches the current driving capability of the driving unit according to a variation in an amount of current required between the auto-zero operation and the amplification operation of the amplifier unit." Claim 21 is dependent from claim 20. The Office Action recognizes that the Signell bias voltage generating circuit is not disclosed as providing the requirement of switching current drive capability in an amount that varies in accordance with requirements of the amplification operation. The Office Action relies upon Curd for teaching this feature, referring to its previous description of Curd in the rejection of claim 1. The Office Action does not set forth how the Signell unit is specifically to be modified. Instead, it is concluded that "it would have been obvious . . . to use the specific 'bias voltage generating circuit' of Curd for the broadly disclosed 'bias voltage generating circuit' of Signell et al. to obtain the expected advantage of efficient dual-mode operation allowing for power savings."

It is submitted that the rejection falls short of the burden for establishing obviousness imposed by the statute and a myriad of legal precedents only some of which have been discussed above. The Office Action lacks identification of the contemplated modification of Signell with the particularity these precedents require. The Office Action does not state why it concludes that a person of ordinary skill in the art would have expected to obtain an advantage over the Signell arrangement by the examiner's proposed modification, or would have expected that a purported advantage of Curd would have been applicable to Signell.

It is submitted, further, that the teachings of Signell and Curd, taken individually or in combination, would not have led an artisan to any modification that would result in the claimed invention. Curd does not teach changing current driving capability of a driving unit according to a variation in an amount of current required for the load or, more specifically, the recitation of claims 11 and 20:

> a control unit which switches the current driving capability of the driving unit according to a variation in an amount of current required between the auto-zero operation and the amplification operation of the amplifier unit.

2. Claim 12

Claim 12 is dependent from claim 11 and additionally requires that the driving unit include a plurality of bias circuits which are connected in parallel and have different current driving capabilities, and that the control unit switches the current driving capability by controlling the number of circuits to operate out of the plurality of bias circuits. Neither Signell nor Curd disclose these additional requirements, nor have they been addressed in the Office Action rejection. Curd does not disclose a control unit that controls the *number* of circuits of the plurality of circuits that operate. It is submitted, therefore, that the rejection of claim 12 fails both for the lack of disclosure in the applied references of all requirements of parent claim 11 and for the additionally recited elements.

3. Claim 13

Claim 13 is dependent from claim 11 and further requires that the driving unit include a plurality of bias circuits which are connected in parallel and have the same current driving capabilities, and that the control unit switches the current driving capability by controlling the number of circuits to operate out of the plurality of bias circuits. Neither Signell nor Curd disclose these additional

requirements, nor have they been addressed in the Office Action rejection. It is submitted, therefore, that the rejection of claim 13 fails both for the lack of disclosure in both references of all requirements of parent claim 11 and for the additionally recited elements.

Curd provides no discussion as to current driving capabilities of the two parallel circuits illustrated in Fig. 2. Whether the driving capabilities are the same or different is of no concern in the Curd disclosure. Curd does not disclose a control unit that controls the *number* of circuits of the plurality of circuits that operate. Assuming, *arguendo*, that "IN" and the inverter comprise a control circuit, this combination would activate one of the parallel circuits while deactivating the other via the inverter. That is, while the circuit to be activated may be controlled, the number of circuits that are activated is not controlled.

4. Claim 14

Claim 14 is dependent from claim 12. The rejection of claim 14 fails with respect to the requirements of its parent claims 12 and 11 for the reasons presented above.

Claim 14 additionally requires that "*each* of the plurality of bias circuits includes . . . a CMOS transistor pair composed of a PMOS transistor and an NMOS transistor which are connected in series between a power supply potential and a ground potential and have a common drain connected to their respective gates, the drain outputting the bias voltage . . . .(emphasis supplied)" This requirement is not addressed in the Office Action, which presumably has relied upon the Fig. 2 disclosure of Curd for the rejection. Fig. 2 does not illustrate a plurality of bias circuits, each including a CMOS pair as required by claim 14. Lack of such disclosure is an additional basis upon which it is submitted that the rejection is untenable.

5. Claim 16

Claim 16 is dependent from claim 14. The rejection of claim 16 fails with respect to the requirements of its parent claims 14, 12 and 11 for the reasons presented above.

Claim 16 additionally requires that the control unit controls the number of circuits to operate by sending control signals to the respective switching elements included in the plurality of bias circuits. Both Signell and Curd lack a teaching or suggestion of this additional feature, another basis for withdrawal of the rejection.

6. Claim 18

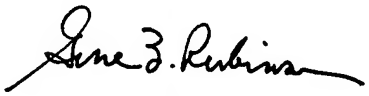
Claim 18 is dependent from claim 11. The rejection of claim 9 fails with respect to the requirements of its parent claim 11 for the reasons presented above.

Claim 18 additionally requires, in part, that the control unit switches the output of the driving unit between a first bias voltage and a second bias voltage according to a variation in the amount of current necessary for the load. Neither Signell nor Curd discloses this feature, nor has this requirement been addressed in the Office Action.

In summary, based upon the arguments submitted supra, Appellant respectfully submits that all rejections imposed under 35 U.S.C. §§ 102 and 103 are not legally viable. Reversal of the rejections is respectfully solicited.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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VIII. CLAIMS APPENDIX

1. A bias voltage generating circuit, comprising: a driving unit which generates a bias voltage to be applied to a predetermined load; and

a control unit which switches a current driving capability of the driving unit according to a variation in an amount of current required for the load in a period for applying the bias voltage to the load.

2. The bias voltage generating circuit according to claim 1, wherein

the driving unit includes a plurality of bias circuits which are connected in parallel and have different current driving capabilities, and

the control unit switches the current driving capability by controlling the number of circuits to operate out of the plurality of bias circuits.

3. The bias voltage generating circuit according to claim 1, wherein

the driving unit includes a plurality of bias circuits which are connected in parallel and have the same current driving capability, and

the control unit switches the current driving capability by controlling the number of circuits to operate out of the plurality of bias circuits.

4. The bias voltage generating circuit according to claim 1, wherein

the predetermined load is an amplifier which is included in an AD converter.

5. The bias voltage generating circuit according to claim 2, wherein

each of the plurality of bias circuits includes:

a CMOS transistor pair composed of a PMOS transistor and an NMOS transistor which are connected in series between a power supply potential and a ground potential and have a common drain connected to their respective gates, the drain outputting the bias voltage;

a switching element which interrupts a feedthrough current occurring from the CMOS transistor; and

a switching element which controls output of the bias voltage from the CMOS transistor.

7. The bias voltage generating circuit according to claim 5, wherein

the control unit controls the number of circuits to operate by sending control signals to the respective switching elements included in the plurality of bias circuits.

9. The bias voltage generating circuit according to claim 1, wherein

the driving unit includes a bias circuit which can output a first bias voltage and a second bias voltage which are different from each other, selectively; and

the control unit switches the output of the driving unit between the first bias voltage and the second bias voltage according to a variation in the amount of current necessary for the load.

11. An amplifier circuit, comprising:

an amplifier unit which repeats an auto-zero operation and an amplification operation alternately;

a driving unit which supplies the amplifier unit with a bias voltage; and

a control unit which switches the current driving capability of the driving unit according to a variation in an amount of current required between the auto-zero operation and the amplification operation of the amplifier unit.

12. The amplifier circuit according to claim 11, wherein

the driving unit includes a plurality of bias circuits which are connected in parallel and have different current driving capabilities, and

the control unit switches the current driving capability by controlling the number of circuits to operate out of the plurality of bias circuits.

13. The amplifier circuit according to claim 11, wherein

the driving unit includes a plurality of bias circuits which are connected in parallel and have the same current driving capability, and

the control unit switches the current driving capability by controlling the number of circuits to operate out of the plurality of bias circuits.

14. The amplifier circuit according to claim 12, wherein

each of the plurality of bias circuits includes:

a CMOS transistor pair composed of a PMOS transistor and an NMOS transistor which are connected in series between a power supply potential and a ground potential and have a common drain connected to their respective gates, the drain outputting the bias voltage;

a switching element which interrupts a feedthrough current occurring from the CMOS transistor; and

a switching element which controls output of the bias voltage from the CMOS transistor.

16. The amplifier circuit according to claim 14, wherein

the control unit controls the number of circuits to operate by sending control signals to the respective switching elements included in the plurality of bias circuits.

18. The amplifier circuit according to claim 11, wherein

the driving unit includes a bias circuit which can output a first bias voltage and a second bias voltage which are different from each other, selectively; and

the control unit switches the output of the driving unit between the first bias voltage and the second bias voltage according to a variation in the amount of current necessary for the load.

20. A pipelined AD converter having a plurality of stages of conversion units which generate several bits of digital values of descending order from an input analog voltage, respectively, the AD converter comprising:

an amplifier unit which repeats an auto-zero operation and an amplification operation alternately;

a driving unit which supplies the amplifier unit with a bias voltage; and

a control unit which switches a current driving power of the driving unit according to a variation in the amount of current required between the auto-zero operation and the amplification operation of the amplifier unit,

the control unit controlling the current driving capability so as to drive at least any one of the plurality of stages of conversion units with a relatively high current and drive the other conversion units with a lower current.

21. The pipelined AD converter according to claim 20, wherein the control unit controls the current driving capability so as to drive the conversion unit at the initial stage with a relatively high current and drive the second and subsequent conversion units with a lower current.

IX. EVIDENCE APPENDIX

No evidence has been submitted of record under 37 CFR 1.130, 1.131 or 1.132.

X. RELATED PROCEEDINGS APPENDIX

No decisions have been rendered in Related Appeals or Interferences.